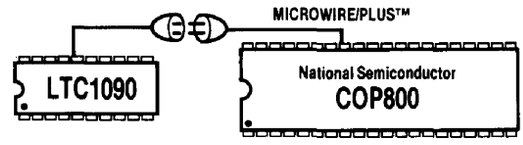
Interfacing the LTC1090 to the COP820C MCU



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Introduction

This application note describes the hardware and software required for communication between the LTC1090 10-bit data acquisition system and the National Semiconductor COP800 microcontroller family which uses the MICROWIRE/PLUS serial interface. The simple four wire interface is capable of completing a 10-bit conversion and shifting the data in 56μs. Configuration of the LTC1090 and the COP820C will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1090 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred in a full duplex format over D_{IN} and D_{OUT}.

The National Semiconductor MICROWIRE/PLUS is a synchronous, full duplex, serial port built into the COP800 family that allows easy interface to the LTC1090. MICROWIRE/PLUS provides clock, data in and data out lines that are compatible with the LTC1090. One additional line (G1) is required to control the $\overline{CS}$ pin on the LTC1090. The schematic of Figure 1 shows how the two devices are connected.

Hardware Description

The actual interface was done using the COP820C, a member of the COP800 family. All code shown here should work with any of the COP800 family.

The code for this interface was developed on a COP820 evaluation board operated in the emulation mode.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer using a 2MHz ACLK. The COP820C clock was 5MHz. To obtain a 56μs transfer time it is necessary to run the COP820C at 20MHz which requires a high speed version of the part.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1090 please see the data sheet.

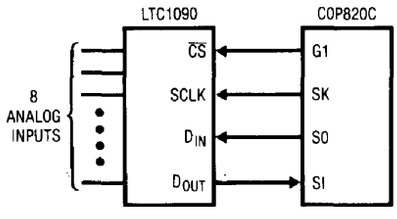

Figure 1. Schematic

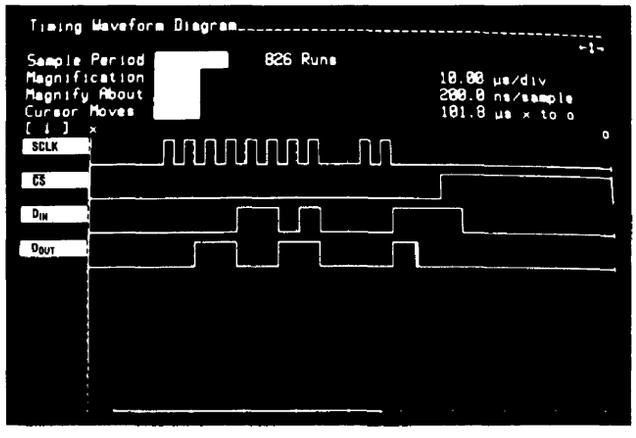

Figure 2. Timing Diagram

Software Description

The software configures and controls the MICROWIRE/PLUS serial interface of the COP820C. Additionally, the software manipulates G1 ($\overline{CS}$ of the LTC1090) and generates a delay during which time the LTC1090 performs a conversion.

The code first loads the LTC1090 D_{IN} word into memory location. $F0. This D_{IN} word configures the LTC1090 for CH0 with respect to CH1, MSB first, unipolar and 10 bits as shown in Figure 3. Next port G is configured for MICROWIRE™ master mode and G1 is configured as an output. The control register is initialized so that SO and SK are outputs. The port G data register address is loaded into the B register. At this point the COP820C is initialized and the data transfer process is ready to begin.

The D_{IN} word for the LTC1090 is then loaded into the ACC from location $F0. G1 ($\overline{CS}$) is cleared and D_{IN} is transferred into the MICROWIRE shift register. The BUSY bit of the PSW register is set which starts the transfer of the first eight bits. A delay consisting of 15 NOPs waits for the data shift to finish at which time the D_{OUT} word from the LTC1090 is loaded into the ACC. The busy bit is set again which causes the transfer to continue. Then, the D_{OUT} word in the ACC is stored in location $F3. The busy bit is cleared which halts the transfer. Two more bits have been shifted at this point. G1 ($\overline{CS}$) is set and the contents of the

0	0	0	0	1	1	0	1
S/D	O/S	S1	S2	UNI	MSBF	WL1	WL0

Figure 3. D_{IN} Word for LTC1090

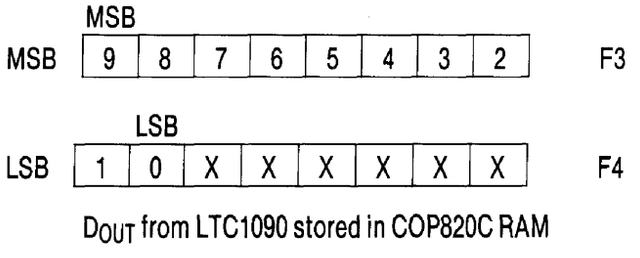

Figure 4. Memory Map

LABEL	MNEMONIC	COMMENTS
	LD (F0)←0D	LOAD 0D INTO F0 (D_{IN})
	LD (D5)←32	CONFIGURE PORT G
	LD (EE)←8	CONFIGURE CONTROL REG.
	LD (B)←D4	PORT G DATA REG. INTO B
LOOP	LD (A)←(F0)	LOAD D_{IN} INTO ACC
	RBIT 1	G1 RESET ($\overline{CS}$ GOES LOW)
	X (A)←→(E9)	LOAD D_{IN} INTO SHIFT REG.
	LD (B)←EF	LOAD PSW REG ADDR IN B
	SBIT 2	TRANSFER BEGINS
	NOP	15 NOPs FOR TIMING
	X (A)←→(E9)	LOAD D_{OUT} INTO ACC
	SBIT 2	TRANSFER CONTINUES
	X (A)←→(F3)	LOAD D_{OUT} IN ADDR F3
	RBIT 2	STOP TRANSFER
	LD (B)←D4	PUT PORT G ADDR IN B
	SBIT 1	G1 SET ($\overline{CS}$ GOES HIGH)
	X (A)←→(E9)	LOAD D_{OUT} INTO ACC
	RC	CLEAR CARRY
	RRCA	SHIFT RIGHT THRU CARRY
	RRCA	SHIFT RIGHT THRU CARRY
	RRCA	SHIFT RIGHT THRU CARRY
	X (A)←→(F4)	LOAD D_{OUT} IN ADDR F4

Figure 5. COP820C Code

MICROWIRE shift register are swapped with those of the ACC. The carry is cleared and the data in the ACC is shifted right, through the carry bit three times. This puts the two LSBs of the D_{OUT} word in the MSBs of the ACC. The contents of the ACC are then stored in $F4. The data at this point is left justified as shown in Figure 4.

44 ACLK cycles must be allowed between transfers for the A/D to perform its next conversion. The instructions, after G1 is set, take enough time so that no additional delay is required by this program.

Summary

A four wire interface between the LTC1090 and the COP820C with a combined data conversion and transfer time of 56μs was demonstrated. The interface used the MICROWIRE/PLUS serial port of the COP820C. The 10 data bits of the LTC1090 are shifted MSB first in one eight bit and one two bit transfer. The data is stored left justified in the COP820C's internal RAM.